FE-D2: Next Steps

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Next Steps for FE-D line, and some issues:

- Discuss what are the next steps, how far should we proceed in our evaluation of FE-D2, do we prepare an FE-D3 and on what timescale, etc.
- Do not discuss steps for other chips in reticle (MCC-D2, DORIC2, VDC2).

Present some thoughts to provoke discussion...

FE-D2 Evaluation

Steps towards complete FE-D2 evaluation:

- Complete wafer characterization of yield, and differences in yield for corner wafers of experimental run.
- Complete characterization of bare die, in terms of analog and digital performance of the design, looking for flaws.
- Irradiate single bare die on rad-hard support cards. Check the behavior during irradiation (SEU) and post-rad (total dose).
- Select good die, and have wafers bumped and assembled into bare modules. Make all standard lab and testbeam measurements of performance.
- Perform irradiations of single chip and 16-chip flip-chipped module assemblies. Look for additional performance issues during and after irradiation.

Steps towards production version of FE-D:

- Next step would be to compile a list of necessary modifications to address whatever issues arise in the evaluation, and then proceed towards an FE-D3 submission, which would be a “pre-production” version of the FE chip.

What have we learned so far from FE-D2 testing

For FE-D2D:

- Observe that known digital problems (buffer sizing, etc.) seem to have been properly fixed.
- Observe similar yield and readout problems to those seen in FE-D1b (backup) run. This means that there are many columns which fail because of “Row 0” problems. The yield of the Pixel Register is similar to FE-D1b. The yield of chips with nine good column pairs is typically 0 per wafer, with at most a few such die per wafer. In all of the FE-D2 probing at LBL so far, there has not been a single “digitally perfect” chip (all pixels in all column pairs working with digital injection).
- There is no apparent (strong) correlation of FE-D2D column-pair yield with the processing corners in the experimental run. This suggests that we continue to have no clues about how to improve this unacceptable yield.
- Conclude: this design in DMILL seems to be a dead-end for us...

For FE-D2S:

- The yield for the digital readout is much better than for the FE-D2D chips. If one uses the loose critieria that a good die has good registers and nine good column pairs (allowing a small number of dead pixels per good column pair), then the yield is about 50%. There are typically a few bad pixels per chip in this sample.
- See only two yield issues correlated with corners. The first is that for large Leff, the Pixel Register yield is reduced. The second is that for small Leff, the number of bad pixels in good column pairs is increased. Since this particular variation is a mask change, and has electrical consequences for device speed, these may be legitimate indications of marginal aspects of our design.

Global Comments:

- The peculiar analog behavior seen in FE-D1 is unfortunately confirmed in FE-D2. The results of threshold scans are seen to fluctuate from scan to scan when hard resets are performed. In addition, there is a significant left-right asymmetry in the average threshold, which does not correlate with the measured values of VCCD and VTH on the two sides of the die, and leads to a dispersion of about 600e.
- This instability is seen in FE-D2S and FE-D2D, and so cannot be related to the readout oscillation problems observed in FE-D2D and FE-D1.
- This probably should be understood, in case it arises from a generic design flaw (which could in principle re-occur in future chips in other processes).

Comments:

- The present FE-D2D design seems to be useless for further investigations, due to the very poor yield for useful chips. We have no idea how to fix these problems at this time. This is the only design we know of that allows us to fit the desired functionality into a 50μ x 400μ pixel in DMILL.
- The present FE-D2S design looks promising in terms of its yield, but the pixel is completely full. It seems there is no significant yield difference between the static and quasi-static Pixel Register versions, so some space could be regained by restoring the FE-D2D design for the pixel control block. Additional space would still need to be found to re-introduce the 3-bit TDAC into the pixel, and the large dispersions we observe in FE-D2S desperately need this trim capability.
- It seems likely that the only way to implement an FE-D3S would be to increase the size of the pixel beyond 400μ, perhaps to 450μ to give a safety margin (16 column pairs per chip) in the layout.

Two choices:

- Go ahead with an FE-D3S with a larger pixel geometry.
- Continue to emphasize FE-I and return to create an FE-D3 only if there are indications of serious problems with the 0.25μ design.
- I clearly favor the latter, but this is open to discussion...

Next Steps

Propose in either case, we continue to do the following:

- Continue to study FE-D2S die in detail in the lab, including also the Analog Test Chip, in order to understand the performance of the design in detail, and make sure there are no mysteries that could come back to haunt us in future chips (even with other vendors).
- Prepare single FE-D2S die for irradiation. We hope to do some first irradiations at LBL in Feb. We should go ahead and do this at the PS also, just to make sure that we really understand how to do these irradiations.
- Send FE-D2 wafers for bump-bonding, perhaps sending three wafers each to AMS and IZM, and saving one for Sofradir if we continue to work with them. We should get roughly one module per wafer with some safety factor.
- Perform irradiations on complete single chip assemblies and complete module assemblies. Although the chips may not be perfect, and we may not make any additional chips with this vendor, still believe that there are many things to be learned.

Propose: do evaluation of all FE-D2 devices as planned, but do not divert any IC design resources from FE-I effort.